KEMPAC SYSTEM

DOCUMENTATION

6502 CENTRAL PROCESSOR CARD

CP-1

1. FEATURES

* 40 I/O lines with handshaking capability and 4 16-bit timers
* 2k RAM on board
* 3 spare IC sockets for max. 24k ROM or 6k extra RAM
* based on 6502 microprocessor
* data, address and control lines buffered for easy expansion
* strap selectable decoding, full 65k address space available
* power-on reset
* auto-reset circuitry for critical applications
* single 5 volt supply
* Eurocard format
* 4k powerful monitor program available
* all IC's in sockets for easy servicing
* layout computer designed

2. BLOCK DIAGRAM

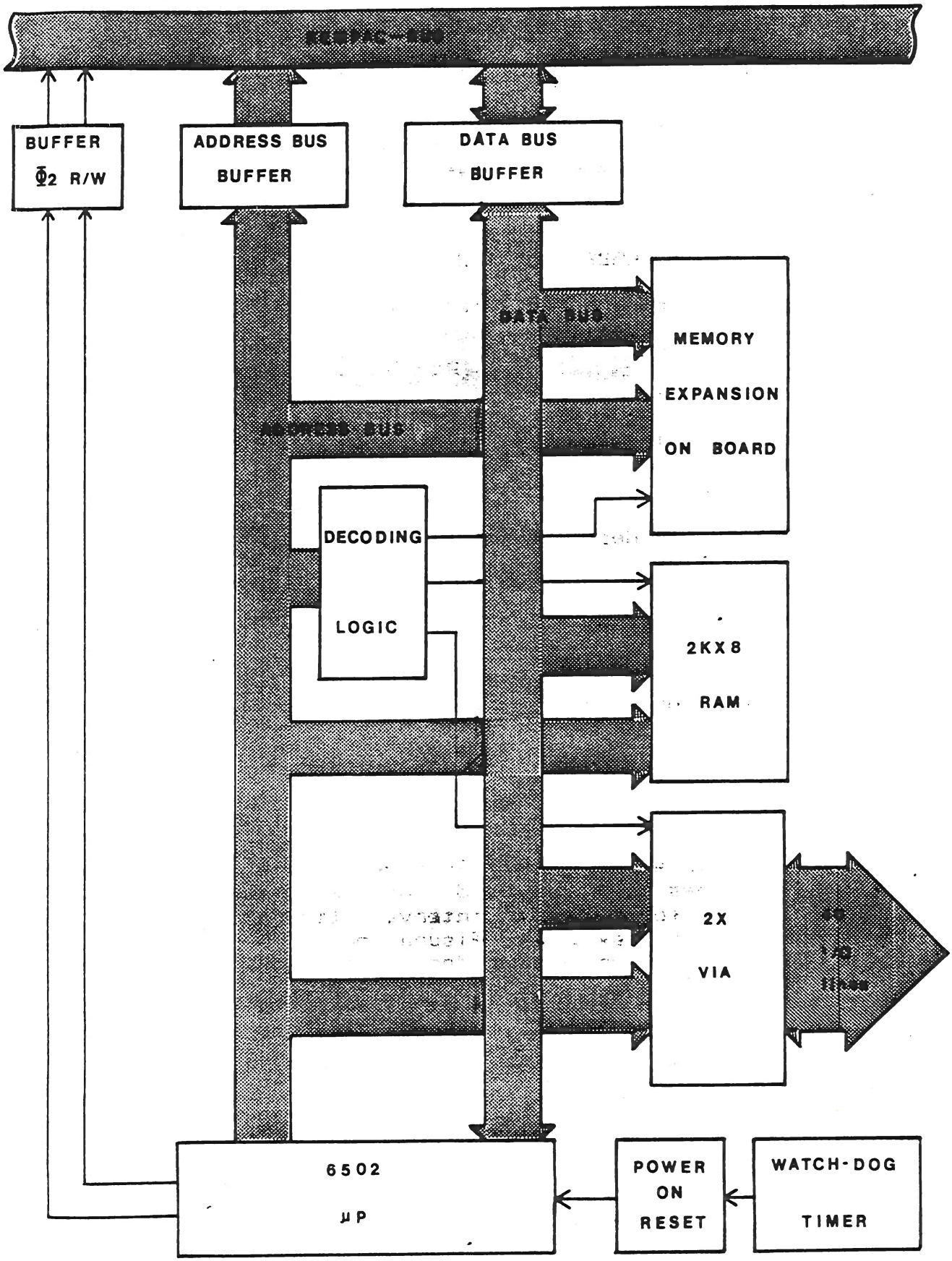


fig. 1

3. Description

The CP-1 card is designed to operate as a stand alone controller card as well as part of the KEMPAC computer system. The card contains (see block diagram fig. 1):

a. 6502 microprocessor with a 1 Mhz X-tal clock

b. two VIA's (6522) for I/O

c. three 28 pins sockets for memory expansion (ROM/RAM)

d. power-on reset circuit

e. watchdog circuit

f. decoding logic

g. data address and control-line buffers

These circuits are described seperately below.

a. 6502 microprocessor

A detailed description is given in a 6502 data sheet.

b. VIA's

The two VIA's provide for 40 programmable I/O-lines; eight of these lines can be used for handshake applications. Together with four 16-bit interval timers and two shift registers, a complex I/O configuration can be realized with a single CP-1 card. For further descriptions of the 6522 refer to the datasheet.

When the KEMPAC-monitor program is used on the CP-1, the I/O-lines are partially used for connection with a Centronics compatible printer, audio load and save hardware, a "bell" and a ASCII-keyboard with a 8x8 matrix. In this case still 10 I/O lines are available for user purposes.

c. Memory expansion

The three spare 28-pins IC-sockets can be used for memory expansion. A wide range of different memory IC's is possible:

EPROMS:	2716, 2516, 2732, 2532, 2732A 2764, 68764
RAM's:	TMM2016 NMOS M58725 NMOS HM6116 CMOS MV5516 CMOS And many more pin compatible types
ROM's:	2316, 2332, 2364 Or pin compatible types

See chapter 4 how selection of the memory IC's is made.

d. Power-on reset circuit

The power-on reset circuit consists of a 555, operating as an one-shot. When power is applied to the CP-1 card, the reset input of the 6502 uP (and the two VIA's) will be held low for approximately 5 msec. A reset is also accomplished by connecting K24a to 0 Volt, generally done by an external switch.

e. Watchdog circuit

The function of the 'watchdog circuit' is to generate a reset pulse every second, unless the user program resets the watchdog circuit within this time. This ensures a restart of the program, when this program should fail, due to an environment with large voltage spikes. Two jumpers select this watchdog mode (JP1 and JP2). To reset the watchdog timer it is necessary to toggle output pin CA2 of VIA 2. REMEMBER THAT YOUR PROGRAM SHOULD RESET THE WATCHDOG TIMER EVERY 450 msec.!!

The circuit is build up around the CMOS IC 4060. This is a 14-stage divider with a reset input. The oscillator frequency is determined by R6, R12 and C3 according to the following formula:

1/(2.2*R6*C3) -when R12=10*R6-

The frequency at output Q12 is calculated:

f(Q12)=1/(2.2*10kOhm*10nF) * 1/(2exp12) = 1.1 Hertz.

T = 1/f = 0.9 sec.

The 4060 will start with all outputs low, so Q12 will go high after 0.9/2 = 0.45 sec.
When jumper JP1 is present, transistor T1 will be turned on so that pin 2 of the 555 will go low. this activates the reset circuit and the program is reentered by the reset vector.

f. Decoding logic

Decoding of the two VIA's and the memory expansion IC7 - IC9 is realized by the IC's 5 and 6 (74LS145). These are 1 of 10 decoders with open collector outputs. This facility allows a 'wired-or' configuration with the output lines. The upper 3 address lines are connected to IC4. This will result a decoding of eight 8K blocks (see drawing). Address lines A12, A11 and A10 are decoded to eight 1K blocks by IC5.

It is possible by making a specific connection in the jumper array to select the VIA's or memory expansion within a specified memory area. The 2Kx8 RAM on board occupies address space from $0000 to $07FF. The 6502 uP needs RAM at location $0000 to $00FF for zero page modes and indirect addressing, and $0100 to $01FF for stack, so the address space of the described 2K RAM area is fixed. For decoding see fig.3 on page 8.

All address and data lines are buffered with the bus transceiver 74LS245 (IC 1,2 and 3). This allows memory expansion in an easy way. Every other KEMPAC-card is buffered too; this eliminates load problems with the address and data bus. The control lines Ø2 and R/W are buffered by IC13 (74LS04) and IC15 (74LS32).

4. EXAMPLES FOR ADDRESS SELECTION

In the schematic drawing and table, numbering is based on a 28-pins IC. If you use a 24-pins IC, BE SURE THAT YOU PUT IT IN THE SOCKET IN THE RIGHT WAY !!(see numbers between parenthesis).

The example on the next page shows a configuration with a 2K EPROM, 4K EPROM, 8K EPROM and 2 VIA's (should you ever want such a configuration!) with a minimum used address space.

In this configuration both VIA's require 1K memory space of which only the first 32 bytes are unique.

5. REMARKS

The CP-1 card is delivered with our standard memory decoding.
specification:

4K EPROM at $F000 - $FFFF

VIA 1 at $E810

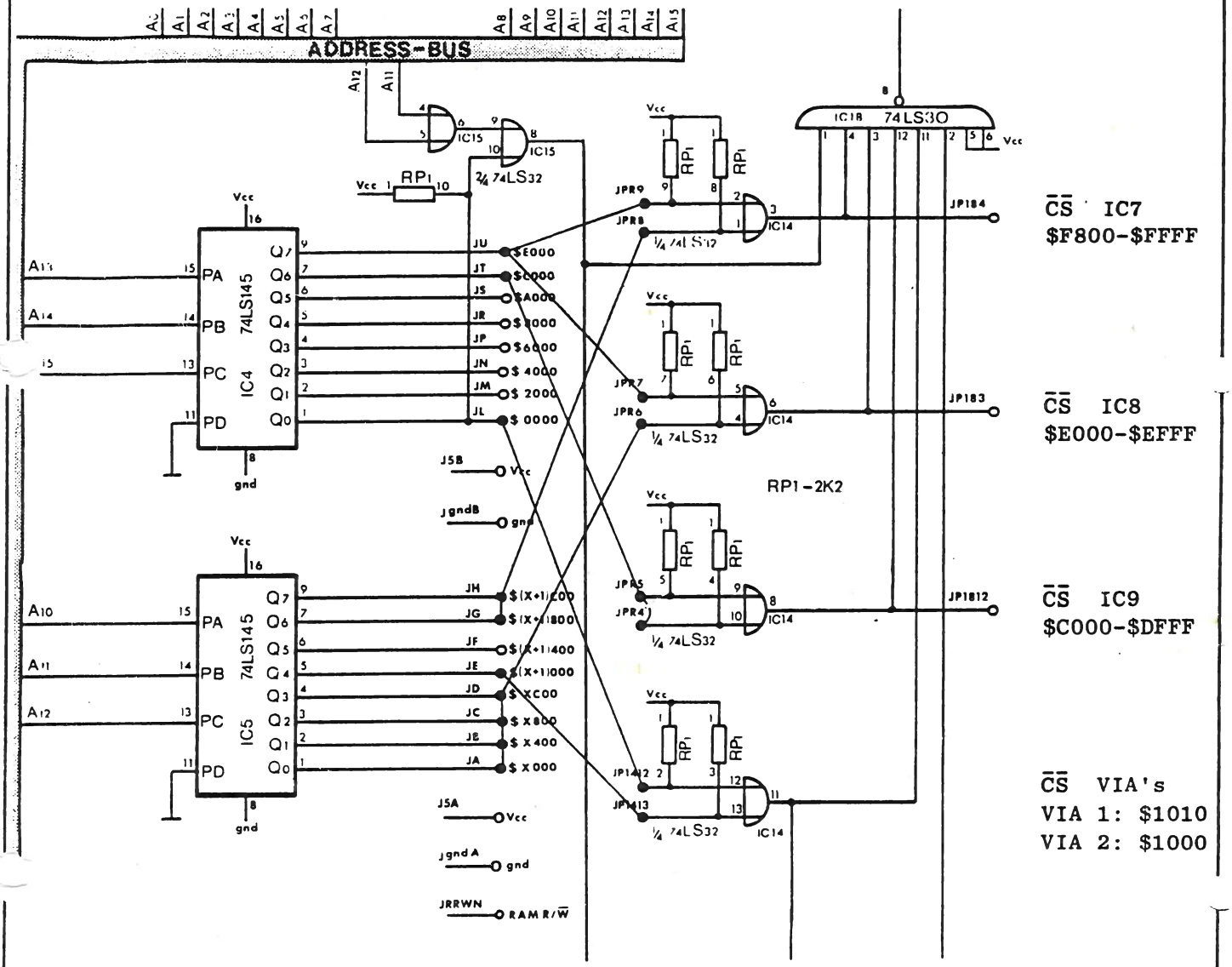
VIA 2 at $E800

This conforms with our monitor program KMON, but can be changed by the user.

NOTE:

When the CP-1 card is used in combination with the VID-2 video-controller card, jumper JP4 must be present. The standard card is delivered with this jumper installed.

DECODING LOGIC (EXAMPLE)



PIN NUMBERS EXPANSION SOCKETS

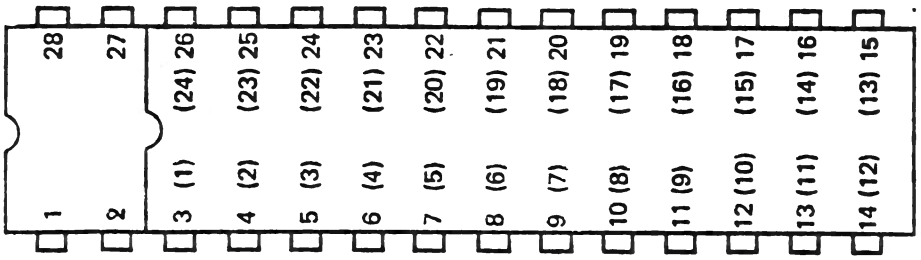
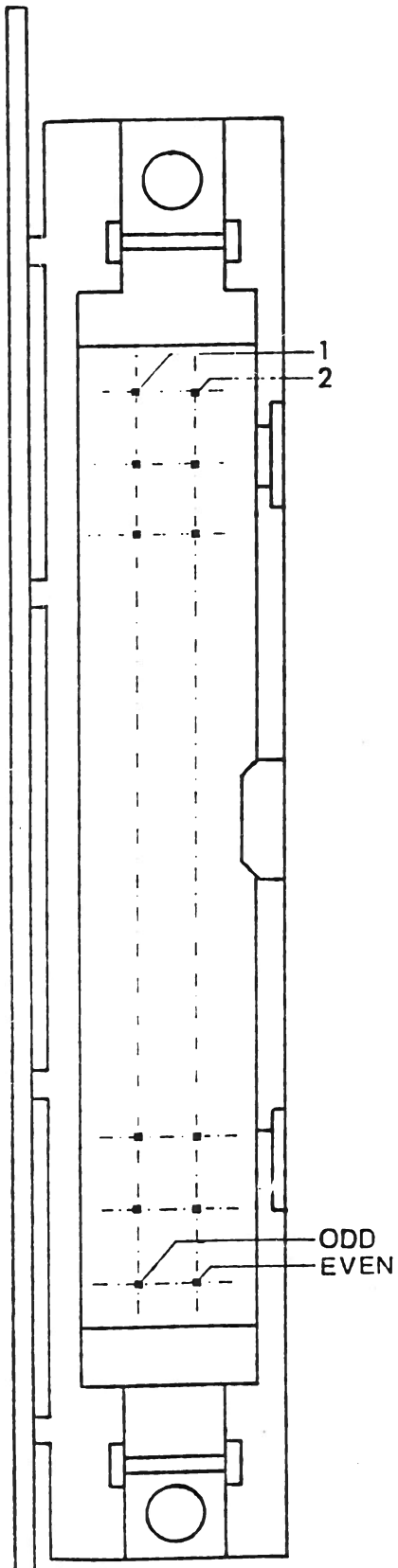


fig. 2

CONNECTIONS FOR VARIOUS TYPES OF MEMORIES:

		JM 1 pin 27(x)	JM 2 pin 23(21)	JM 3 pin 22(20)	JM 4 pin 20(18)	JM 5 pin 2(x)
EPROM	2716 2Kx8	not used	J5 A/B (Vpp)	JGND A/B ($\overline{OE}$)	JP18 12/3/4 ($\overline{CE}$)	not used
	2732 4Kx8	not used	JA11 (A11)	JGND A/B ($\overline{OE}$)	JP18 12/3/4 ($\overline{CE}$)	not used
	2532 4Kx8	not used	J5 A/B (Vpp)	JP18 12/3/4 (PD)	JA11 (A11)	not used
	68764 8Kx8	not used	JA12 (A12)	JP18 12/3/4 ($\overline{CE}$)	JA11 (A11)	not used
	2564 8Kx8	JP18 12/3/4 ($\overline{CS2}$)	JA12 (A12)	JGND A/B (PD)	JA11 (A11)	JGND A/B ($\overline{CS1}$)
	2764 8Kx8	J5 A/B ($\overline{PGM}$)	JA11 (A11)	JGND A/B ($\overline{OE}$)	JP18 12/3/4 ($\overline{CE}$)	JA12 (A12)
RAM	2Kx8	not used	JRRWN ($\overline{WE}$)	JGND A/B ($\overline{OE}$)	JP18 12/3/4 ($\overline{CE}$)	not used
	4Kx8	JPRRWN ($\overline{WE}$)	JA11 (A11)	JGND A/B ($\overline{OE}$)	JP18 12/3/4 ($\overline{CE}$)	not used
	8Kx8	JPRRWN ($\overline{WE}$)	JA11 (A11)	JGND A/B ($\overline{OE}$)	JP18 12/3/4 ($\overline{CE}$)	JA12 (A12)

fig. 3



PIN	FUNCT.	DESCR.	PIN	FUNCT.	DESCR.
1	GND		2	+5V	
3	2PA0	column 1	4	1PA0	row 1
5	2PA1	column 2	6	1PA1	row 2
7	2PA2	column 3	8	1PA2	row 3
9	2PA3	column 4	10	1PA3	row 4
11	2PA4	column 5	12	1PA4	row 5
13	2PA5	column 6	14	1PA5	row 6
15	2PA6	column 7 beep enab	16	1PA6	row 7
17	2PA7	column 8	18	1PA7	row 8
19	2CA2	WDT JP2*	20	1CA2	tape out enable
21	2CA1	not used	22	1CA1	not used
23	n.c.		24	set overflow	not used
25	n.c.		26	n.c.	
27	n.c.		28	n.c.	
29	2CB1	user I/O	30	1CB1	printer acknowl.
31	GND		32	+5V	
33	2PB0	user I/O	34	1PB0	printer D0
35	2PB1	user I/O	36	1PB1	printer D1
37	2PB2	user I/O	38	1PB2	printer D2
39	2PB3	user I/O	40	1PB3	printer D3
41	2PB4	user I/O	42	1PB4	printer D4
43	2PB5	user I/O	44	1PB5	printer D5
45	2PB6	user I/O	46	1PB6	printer D6
47	2PB7	CRTcontrol K13a JP4*	48	1PB7	printer D7
49	2CB2	IRQ ackn. K17c JP3*	50	1CB2	printer data str.

*= jumper option: JP = jumper number
K = KEMPAC bus

BOARD LAY-OUT AND LOCATION OF JUMPERS

Watch dog

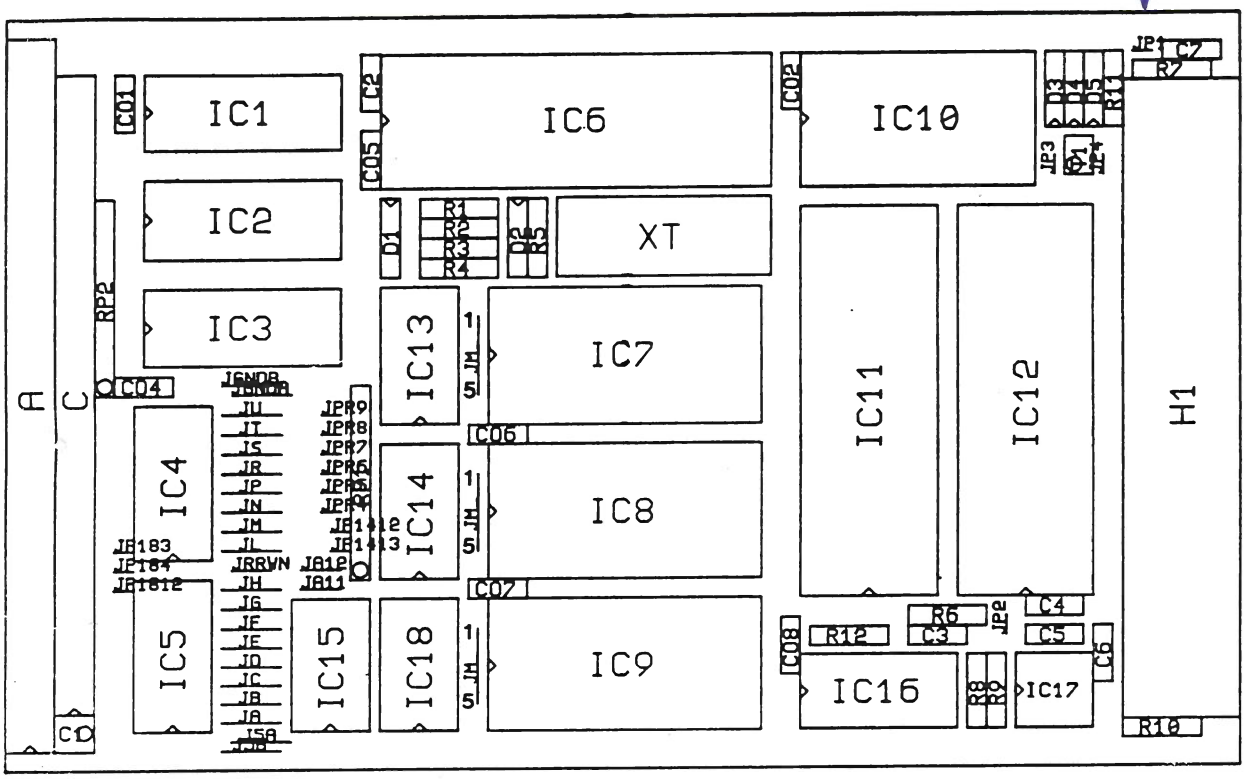
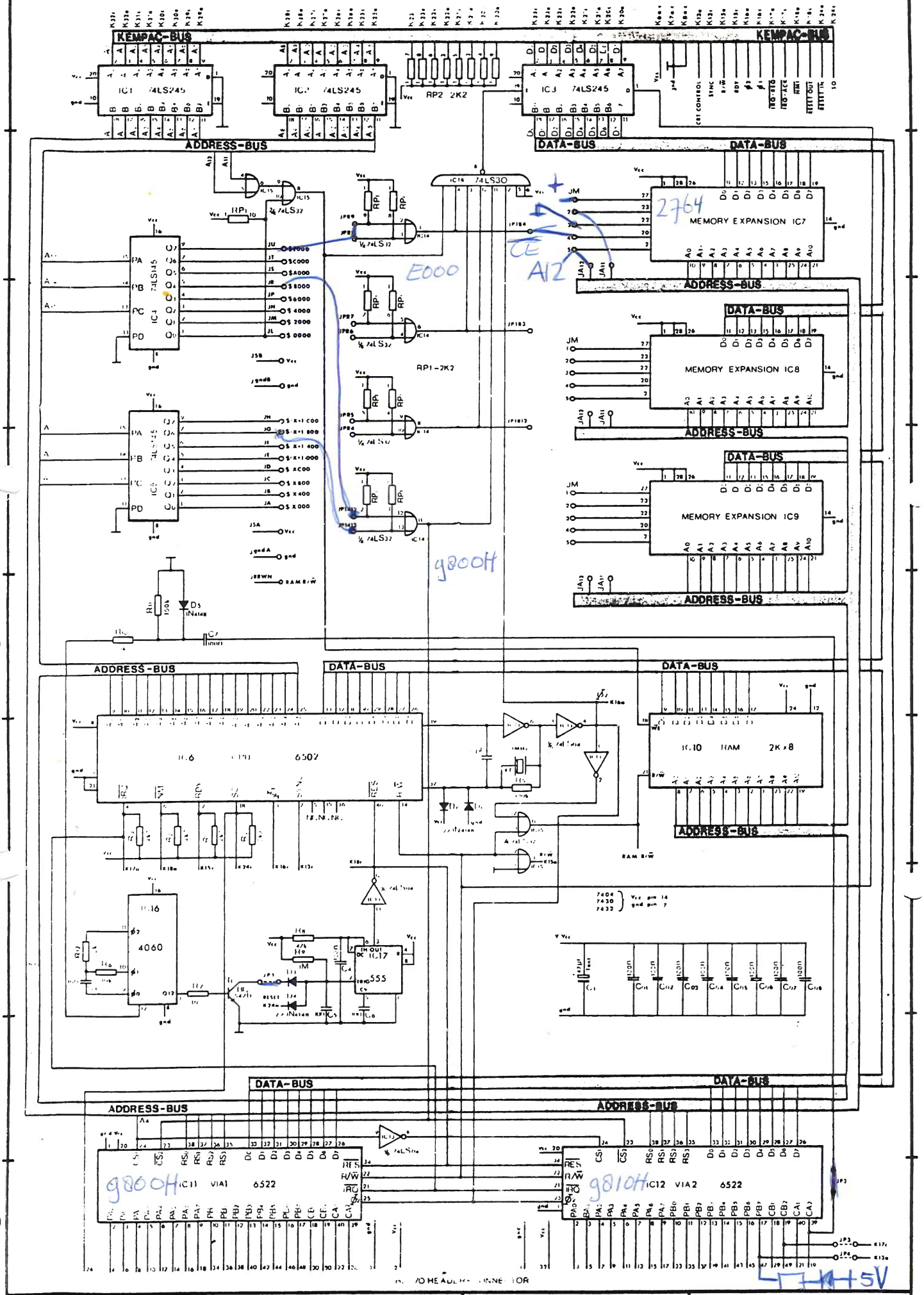


fig. 4



KEMPAC

rev

CP-1

KEMPAC SYSTEM

SUGGESTED MEMORY-MAP

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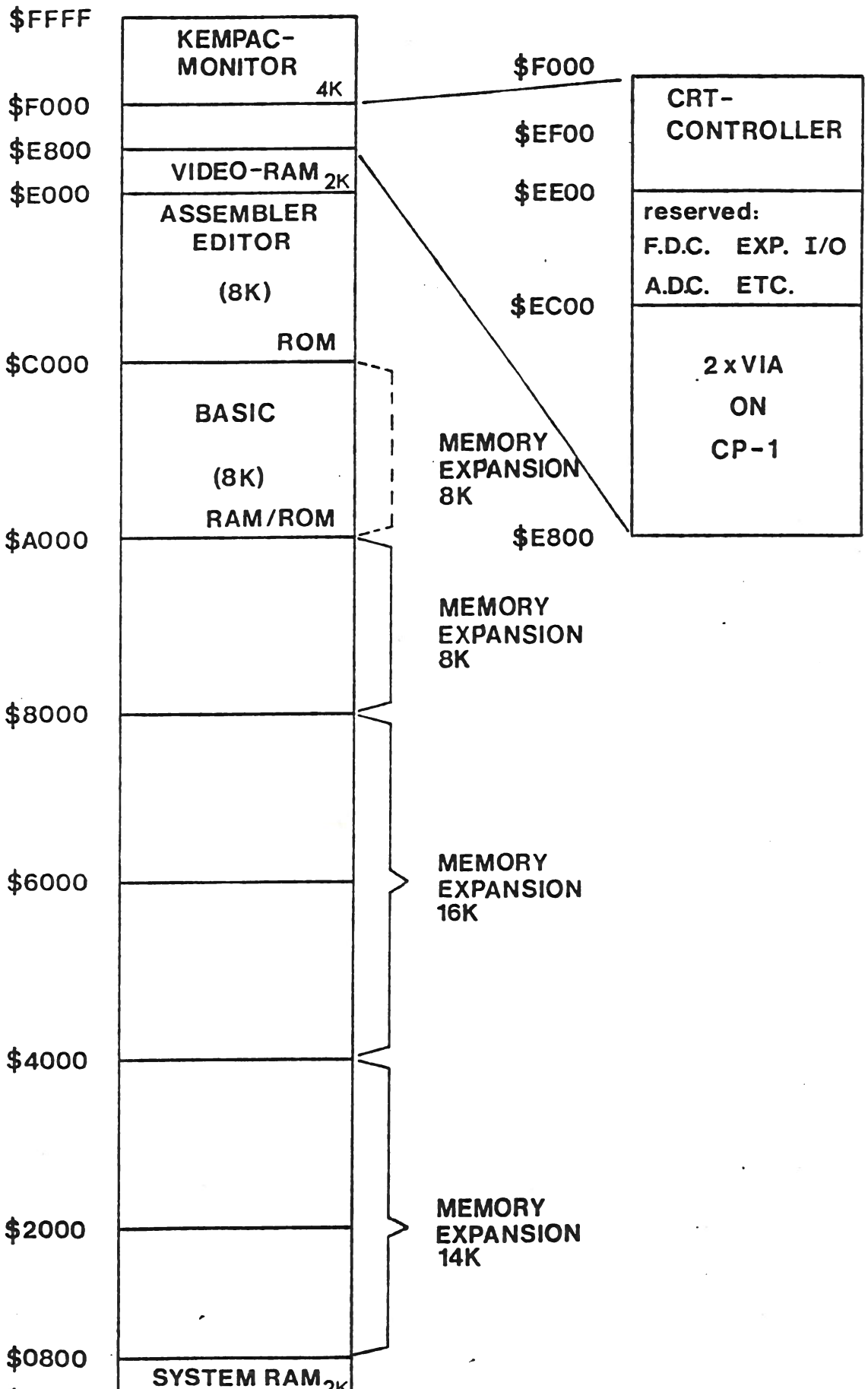
Date: 4-6-1982



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BUS-STRUCTURE

Page:
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Date: 2-6-1982

PIN	A	C
1	~A	~A
2	~B	~B
3	$\overline{\text{PWRFAIL}}$	+5V BAT
4	+12V	+12V
5	-12V	-12V
6	+5V (Vcc)	+5V (Vcc)
7	GND	GND
8	GND	GND
9	P0	P1
10	P2	P3
11	P4	P5
12	P6	P7
13	CRT CONTROL	SYNC
14		
15	R/$\overline{\text{W}}$	RDY
16	Ø2	Ø1
17	$\overline{\text{IRQ-REQ}}$	$\overline{\text{IRQ-ACK}}$
18	$\overline{\text{NMI}}$	$\overline{\text{RESET OUT}}$
19		
20	D7	D6
21	D5	D4
22	D3	D2
23	D1	D0
24	$\overline{\text{RESET IN}}$	S.O.
25	A15	A14
26	A13	A12
27	A11	A10
28	A9	A8
29	A7	A6
30	A5	A4
31	A3	A2
32	A1	A0

DIN 41612 64POL-A,C